EE/CprE/SE 491 WEEKLY REPORT 08
Nov 12 – Nov 18

Group number: **22**

Project title: **ReRAM Compute Asic Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**
  - This week, we continued working on the module designs and testbenches. We are now keeping in mind what we want to understand and present for the design presentation that is fast approaching. We are also working on prioritizing module pins and exploring the constraints of the harness that our designs and other teams' designs are going to be included on together.
- **Past week accomplishments**
  - Vinicius Malaman Soares: Got the ReRAM to simulate. Created a 2x2 ReRAM Crossbar schematic and simulated the schematic with different voltages.
  - Tyler Kloser: Continued to create different characterizations for primary goals for our requirements. Simulate the ReRAM cell.
  - Ali Mannan: Further investigated the characteristics of the ReRAM module of the PDK, helped Vinicius get his ReRAM simulation to work. Created new testbenches and catalogued simulation results, for the 1T1R, as well as some crossbars. Simulated the setting, resetting, and sequential reads and writes of the ReRAM.
  - Austin Miller: Compared some 1S1R options (area of nearly all are bigger than the standard 1T1R). Explored the constraints of the Caravel harness (# of pins, muxing, control)
- **Pending issues**
  - Tyler Kloser: N/A
  - Ali Mannan: N/A
  - Austin Miller: Details of the harness and constraints are not straightforward; I may need to simply bring the harness into the schematic and layout to get a better idea
  - Vinicius Malaman Soares: N/A

- **Individual contributions**

NAME	Individual Contributions	Hours this week	HOURS cumulative
Tyler Kloser	Characteristics for primary goals, simulate ReRAM	5	48
Ali Mannan	Characteristics of ReRAM cells, simulation and testing of ReRAM module	6	58
Austin Miller	Caravel exploration, 1S1R comparisons	4	61
Vinicius Malaman Soares	1T1R simulation working. 2x2 ReRAM crossbar simulation.	5	53

- **Comments and extended discussion**
  - N/A

Plans for the upcoming week

- Ali Mannan: Completely finish all relevant simulations of ReRAM. Begin layout work on 1T1R/ReRAM crossbars with LVS/DRC passing.
- Tyler Kloser: Understand ReRAM simulation and keep working on specific characteristics
- Austin Miller: Discuss constraints and problems with Jason Xie from a previous team and how he implemented the 4x4 crossbar on the latest tapeout. Prioritize pin locations and routes (internal vs external).
- Vinicius Malaman Soares: Work on getting the presentation for the design review panel started. More ReRAM simulations according to weekly meeting.

- **Summary of weekly advisor meeting**
  - Much of this week's meeting was spent discussing the new 1S1R device and whether it would be useful to pursue and add to our test devices. We discussed possibly doing a simpler 1S1R module or moving forward with the proposed one, but ensuring that we would create at least a 2x2 structure with it. We then discussed the results of 1T1R schematic simulations, which look good so far. We discussed a little further what other tests should be run in the testbench for the 1T1R, too. Specifically, showing the ReRAM module can be written to (set or reset), and read. We discussed the design presentation that is coming towards the end of the semester and what it will entail for us. These were mostly key considerations for the presentation, including what the faculty may ask us about, what we should try to avoid, and other important points to be aware of.